IN THE SPECIFICATION:

Please amend the paragraph beginning on line 7 of page 1 as follows:

In chip designs in use today, multiple processors may be formed on a single die, along with other circuitry, such as on-board cache, I/O logic and connectors at the edge of the chip, and I/O controllers controlling the flow of data between the I/O interfaces and the processors. For instance, in a typical system in use today as shown in Figure 1, a number of processors (such as the four processors ~~20-50~~ 10-40 shown) are formed on a die, along with crossbar circuitry 60 coupling the processors to input-output controllers (IOCs) 70-90. The IOCs communicate with I/O interfaces 160 ~~100-150~~, with one IOC coupled to each pair of I/O interfaces, as shown.

Please amend the paragraph beginning on line 9 of page 7 as follows:

In the embodiment of Figure 2, if $x = 4$ then $z = 2x$, and such a fully redundant highly available ~~HA~~ system is presented (for a system requiring a three-processor chip), with appropriate implementation of hardware and software control. For critical settings, the multiplier can be higher; e.g. the designer could choose $z = 3x$ or in general $z = Mx$ (or $y = Mx$), where M can be any number greater than or equal to one. M need not be an integer, as long as the product Mx is an integer or is rounded to an integer (i.e., the number ~~of~~ of processors or other elements to be fabricated is a whole number).

Please amend the paragraph beginning on line 14 of page 8, as follows:

If IOC 315 were also to fail, then control circuit would provide IOC 310 ~~300~~ with connections and responsibility for both interfaces 350 and 355, while IOC 320 would take over all I/O tasks for interface 360.